

Overview

The SPI to AXI Bridge IP core is commonly used as a monitor interface to allow external devices to access the internal AXI bus.

A SPI to AXI Bridge provides read/write access by an external SPI device to the various memories and registers that are present in the chip's internal AXI subsystem via an AXI Master component interface. The Bridge converts SPI transactions into AXI Read or Write instructions, allowing the external SPI device to have full access to all memory mapped devices present in the AXI subsystem.

The SPI to AXI Bridge consists of a low-level SPI interface and a SPI protocol layer, and several dual-clock synchronizers.

The low-level SPI interface is clocked by the SPI bus clock (provided by the external SPI device), and is responsible for several things including:

- Serializing the MISO data going to the external device
- Creating synchronizing pulses to the system so that the system can sample (parallel) data from the serializer when it is stable
- De-serializing the MOSI data coming from the external SPI device.

The SPI protocol layer is clocked by the (fast) system clock. The SPI protocol layer is responsible for several things including:

- Interpreting commands from the low-level SPI interface (R/W, address, mode, protection, burst length)
- Generating an AXI Read Address + Read Data / Write Address + Write Data + Write Response transaction based on the command received from the SPI interface
- Presenting (parallel) address and write data from the low-level SPI interface to the system
- Presenting (parallel) read data from the system to the low-level SPI interface

Features

- AMBA® AXI Monitor
- Allows external devices to access the internal AXI Bus
- AXI Master component Read/Write capability
- Useful for updating device software from an external device
- Useful for reading internal memory mapped registers and memory

Deliverables

- Verilog Source
- Complete Test Environment
- SPI Bus Functional Model

