AXI Performance Subsystem - ARM Cortex A5

SILVACO

The AXI Performance Subsystem is an AMBA® AXI4 based system that is useful as the digital infrastructure for building SOCs needing high performance. This system contains an 8 Master component, 16 Slave component AXI4 multi-matrix for supporting multiple high speed user AXI Master components while providing high performance with Cortex-A5 class processors.

Additionally, the subsystem includes four DMA controllers for easily moving data from user peripherals to the "interleaved" internal SRAM controller for the highest contiguous SRAM performance possible.

Closely coupled Instruction and Data SRAM are available to the CPU as independent AXI multi-matrix Slave components with high priority.

The AXI Performance Subsystem includes a standard set of peripherals and cores that supports RTOS and software kernels. Included is a QSPI, serial flash controller for boot loading program images or operating as an Execute in Place (XIP) engine using non-volatile external flash memory with low power.

The AXI Performance Subsystem is soft IP that can be used in all the popular semiconductor technology nodes.

Features

- High Performance
- Linux Support
- RTOS/Kernel Support
- AMBA AXI4 Multi-layer Fabric
- AMAB APB 3.0
- Internal Interleaved SRAM Controller
- QSPI Serial Flash Controller
- Standard APB Peripherals

Applications

- Gateways / Routers
  - Automotive, IoT, Wireless
- Medical
  - Instrumentation / Display
- Home / Office
  - Surveillance / Monitoring / Home Automation
- Industrial
  - System Controllers, Analysis
- Avionics / Military
  - Displays, Communications

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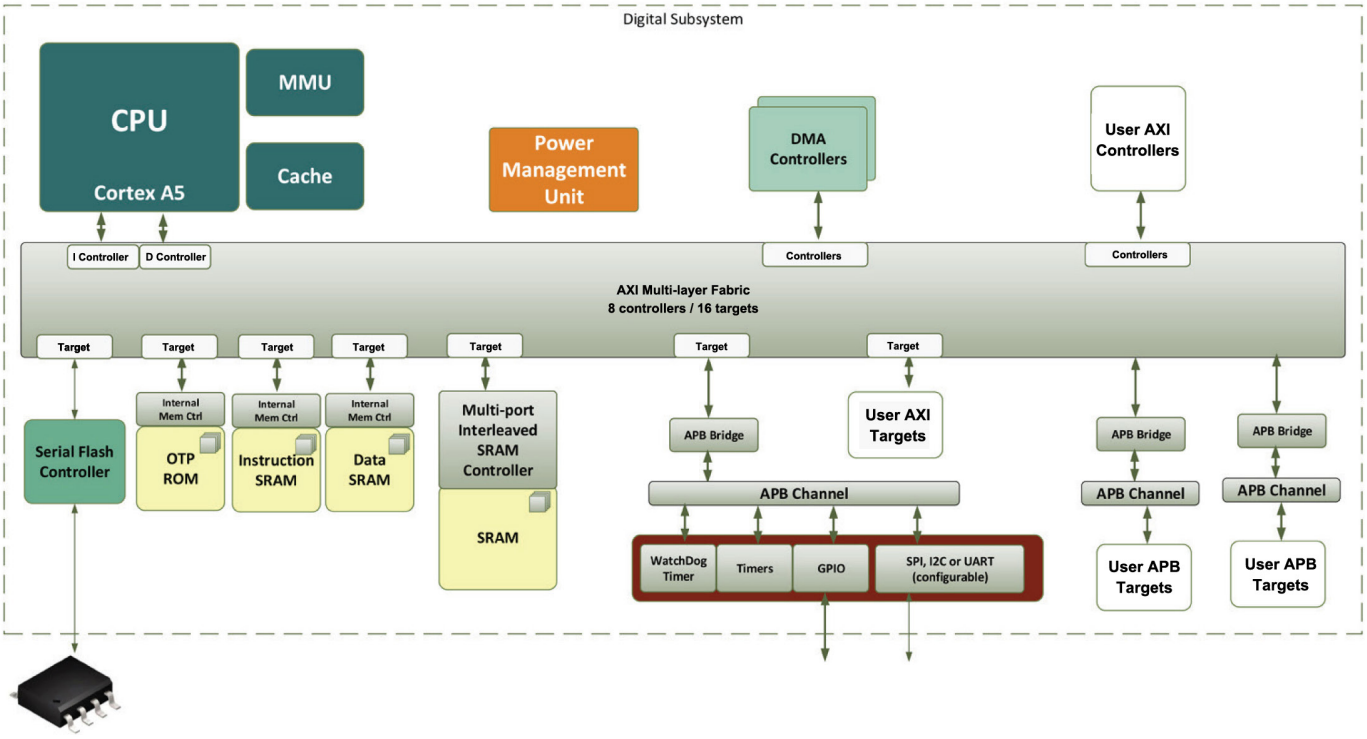

Processor Options

• ARM Cortex-A5

Infrastructure

- AXI4 Multi-layer Fabric
- 8 Master components – 16 Slave components
- APB 3.0 Bus Channel / Decode
- AXI to APB Bridge (3)

IP Cores

- Power Management Unit
- 8, 16, 32-bit Internal SRAM Controller
- Internal Interleaved SRAM Controller
- DMA Controller (4ch)
- QSPI Serial Flash Controller with Execute in Place (XIP)
- Watchdog Timer, Timers (2), GPIO
- Configurable
  - I2C Master component, SPI Master component / Slave component, 16550 UART

Software

- Startup and Interrupt code
- Example Boot Loader from QSPI Serial device
- Example test code for all IP Cores
- Low power example project

Deliverables

• Verilog RTL source code

• Test bench with test suites

• Documentation including User's Guide and Integration Guide

• Technology-independent synthesis constraints

For more information, please contact us at ip@silvaco.com.

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