

# SPI to AHB Lite Bridge

The SPI to AHB Lite Bridge IP core is commonly used as a monitor interface to allow external devices to access the internal AHB bus.

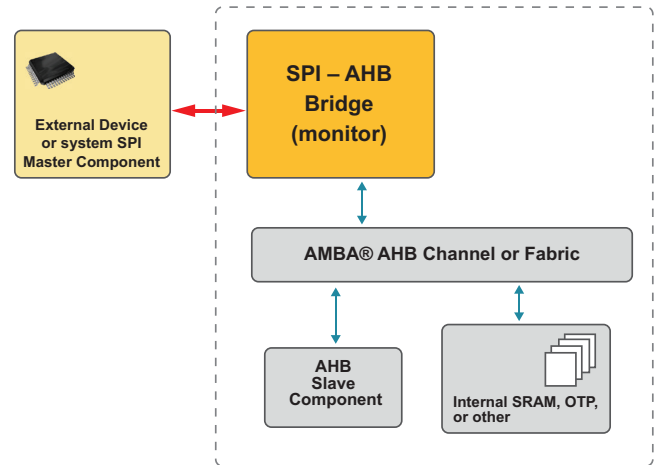
A SPI Slave component to AHB-Lite Interface block provides read/write access by an external SPI device to the various memories and registers that are present in the chip's internal AHB-Lite subsystem. The Bridge converts SPI transactions into AHB Read or Write instructions, allowing the external SPI device to have full access to all memory mapped devices present in the AHB-Lite subsystem.

The SPI protocol layer is responsible for several things including:

- Interpreting commands from the low-level SPI interface (R/W, address, mode, protection, burst length)
- Generating an AHB Read or Write transaction based on the command received from the SPI interface
- Presenting (parallel) address and write data from the low-level SPI interface to the system
- Presenting (parallel) read data from the system to the low-level SPI interface

## Features

- AMBA® AHB Monitor
- Allows external devices to access the internal AHB Bus
- AHB Master Read/Write capability
- Useful for updating device software from and external device
- Useful for reading internal memory mapped registers and memory



## Deliverables

- Verilog Source
- Complete Test Environment
- SPI Bus Functional Model

For more information, please contact us at [ip@silvaco.com](mailto:ip@silvaco.com).