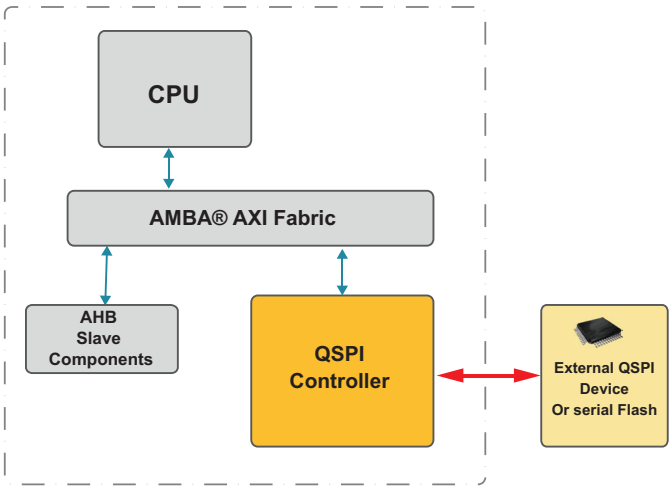
AXI Quad SPI Controller with Execute in Place (XIP)

Overview

Silvaco's Ultra High-Speed cache memory is an adaptable, independent, non-coherent cache Intellectual Property (IP) featuring an advanced cache architecture. This architecture enhances system performance, scalability, power efficiency, data locality, application responsiveness, cost optimization, and market competitiveness, providing a distinctive business value.

Features

- AMBA AXI interface
- Execute-in-place (XIP) functionality for several industry-standard FLASH devices
- DMA Interface
- Software programmable Master component or Slave component mode
- Software programmable SCLK rate for Master component mode
- Quad and Dual-bit mode operation
- 4-bit to 32-bit serial transmit & receive – 1 bit increments
- Full and Half operation
- Separate SCLK input for Master component Mode
- 8 to 256 word Transmit and Receive FIFOs - configurable
- Asynchronous Slave component Interface
- Interrupt control
- LSB or MSB mode
- Up to 4 Slave components under Master component control



Deliverables

- Verilog Source
- Complete Test Environment
- AXI Bus Functional Model

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Rev 041824_0
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