SILVACO

# Parasitic Extraction

## Full Chip and Cell Level RC Extraction

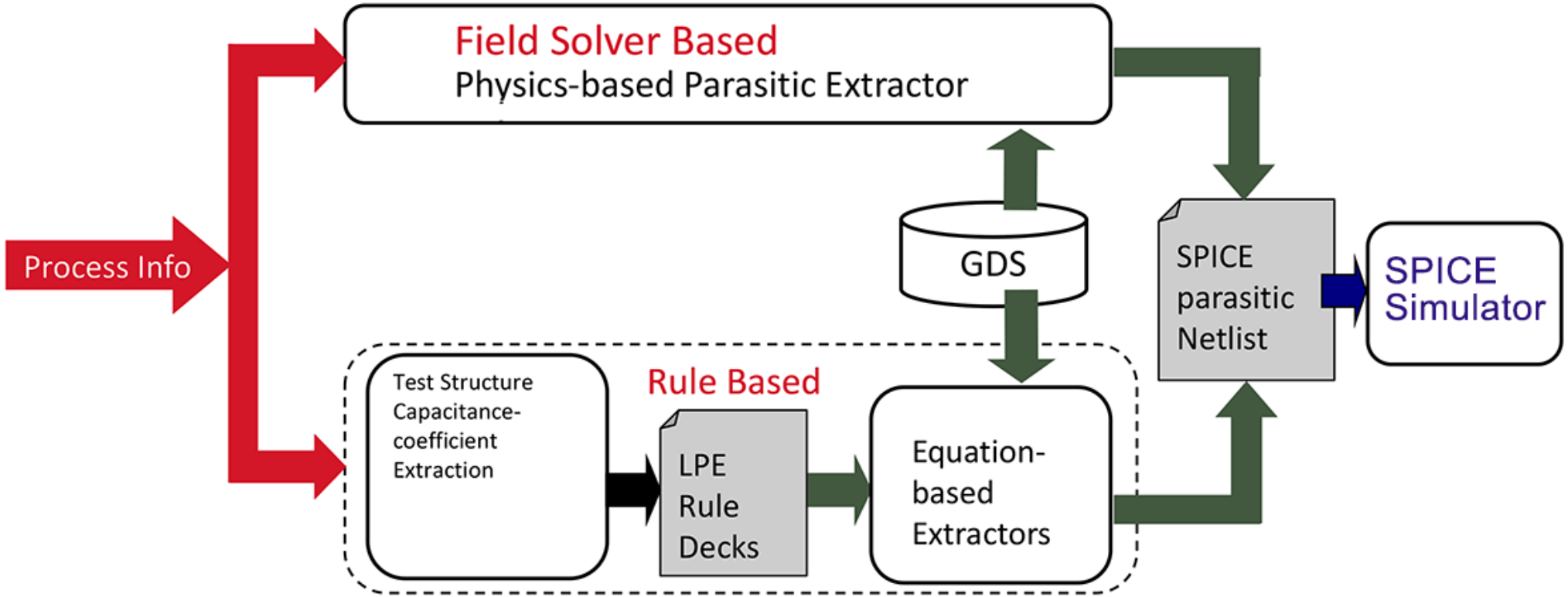
# Contents

# Introduction

- Many solution methodologies for RC extraction (RCX)
- Optimize solution methodology for each application
- A common platform maximizes user choice
- Consider intended user skill set, CAD versus TCAD
- Consider size and topology, versus simulation speed
- How much accuracy is really needed
- User choices are often technology dependent

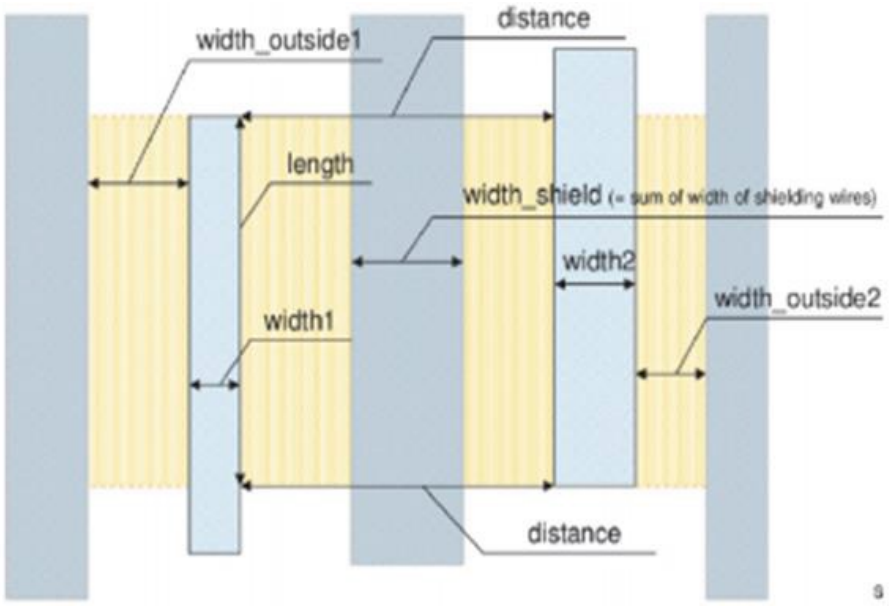
# Solution Methodologies

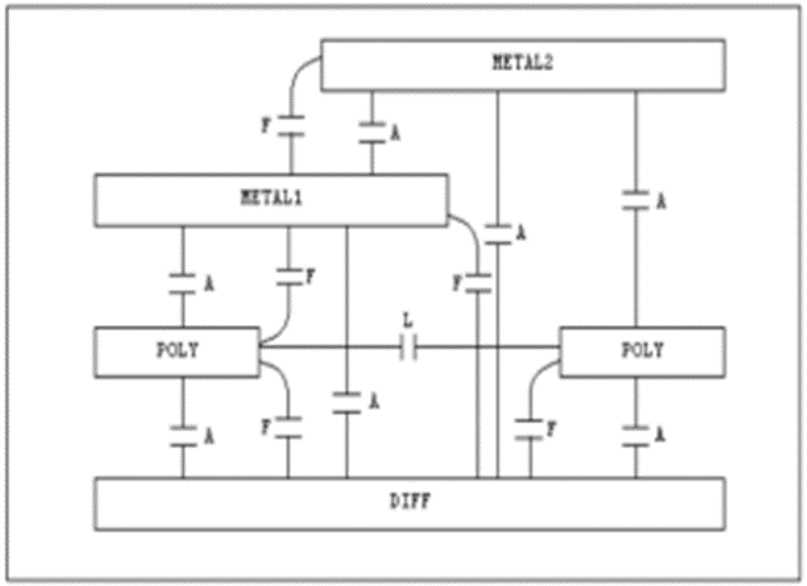
- Rule based (fastest) or Field solver based (most accurate)



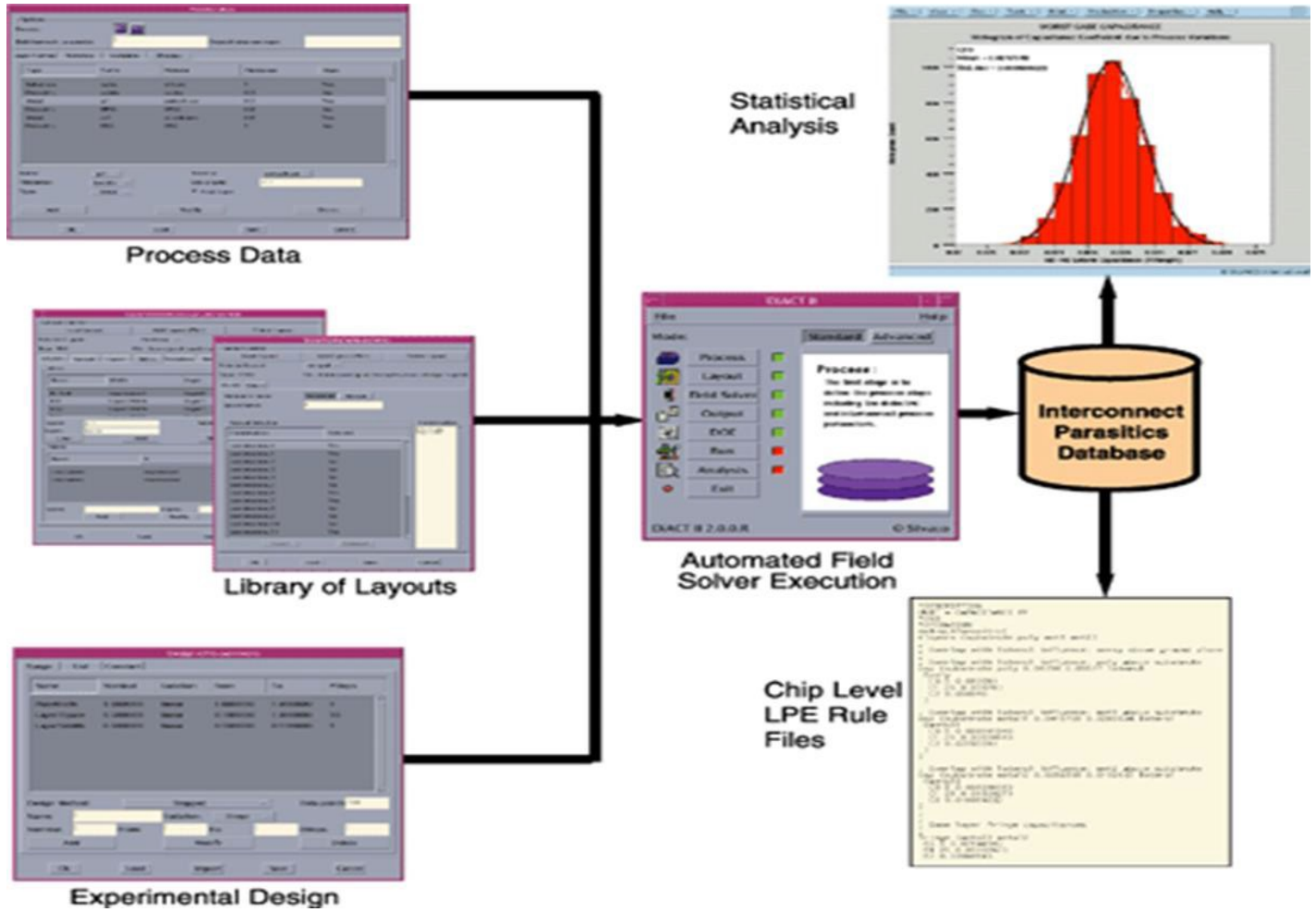
# Rule Based

- Capacitance extract geometry from layout polygons
- Resistance count conductor length in “squares”
- Coefficient database converts polygons into C & R values



# Parasitic Database Generation



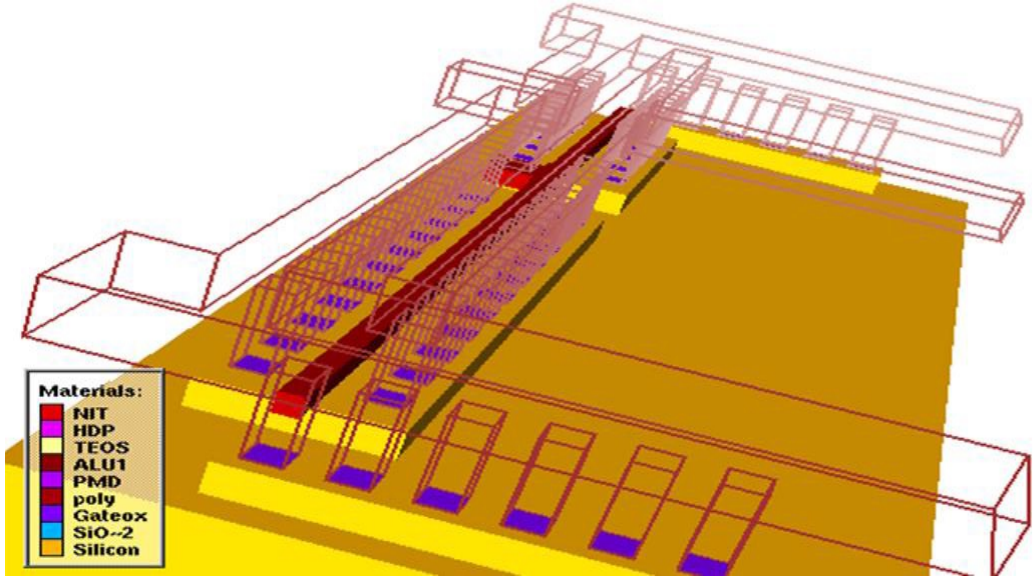

- Generating the capacitance coefficient database for rule based extraction
- requires a field solver
- One time per technology
- Silvaco ‘Exact’ tool

# Field Solver Methods

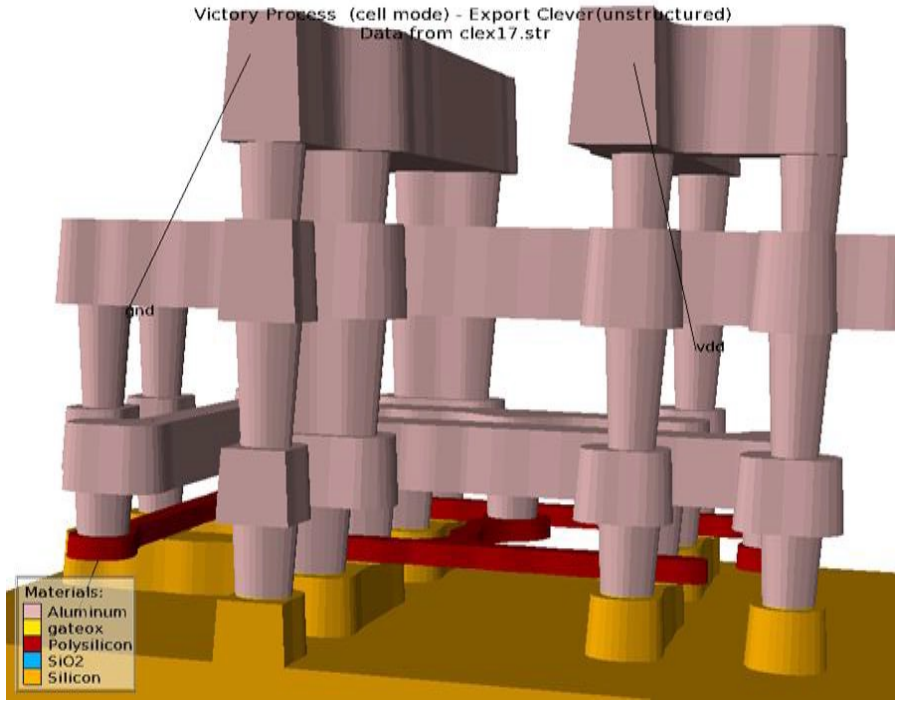
- Field solver's have several methods to apply the physics to the physical representation of the structure
- Field solvers extract both capacitance and resistance
- Finite Difference and Finite Element Methods are:
  - Optimal for complex and curved 3d shapes
- Boundary Element and Random Walk Methods are:
  - Optimal for squared off "Manhattan" shapes
- Simulation speed versus shape complexity trade off
- Silvaco tools use field solvers from both categories

# Boundary Element or Finite Element?

- For uniform layer thickness and Manhattan shapes
  - Boundary Element Method

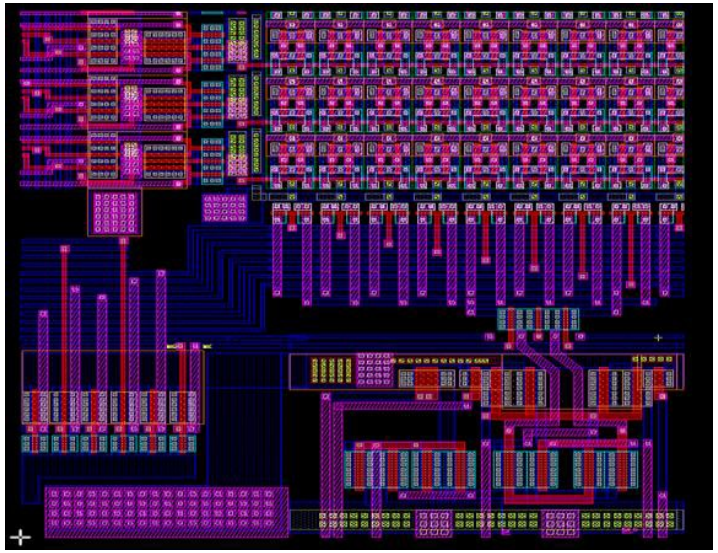



- For complex 3D shapes
  - Finite Element Method



# Summary

- Rule based extraction used for most of the full chip
- Field solver based extraction for complex R & C layout
- Highest accuracy is required for critical cells
- Mix and match techniques within one design



Typical maximum cell size illustration for using field solver techniques